WHAT IS CLAIMED IS:

1. An integrated circuit device having a semiconductor substrate, comprising:

a memory cell array comprising a plurality of volatile memory cells; and

a metal oxide semiconductor field effect transistor (MOSFET) configured as a non-volatile electrically erasable programmable read only memory (EEPROM) device having a floating gate and a control gate, and adapted to store status information associated with the memory cell array,

wherein the MOSFET has a single polysilicon film for the floating gate, and the control gate is disposed within a well in the semiconductor substrate.

2. The device as claimed in 1, wherein the control gate of the MOSFET corresponds to a second conductive ion-implantation region which is spaced from a channel region of the MOSFET and which is formed under the single polysilicon film.

3. The device as claimed in 2, wherein the MOSFET is an n-channel MOSFET, and a program operation for electrically programming the EEPROM is performed by injecting electrons into the floating gate through a hot electron injection

method.

4. The device as claimed in 3, wherein an erase operation for the EEPROM is performed by discharging the electrons captured by the floating gate through an F-N (Fowler-Nordheim) tunneling process.

5. An integrated circuit device having a semiconductor substrate, comprising:

a memory cell array comprising a plurality of volatile memory cells;

at least one redundancy volatile memory cell; and

an electrically programmable non-volatile memory cell configured as a fuse device to identify whether a corresponding one of the memory cells is defective and should be replaced with the redundancy memory cell.

6. An integrated circuit device, comprising:

a plurality of volatile memory cells;

a redundancy memory cell; and

a defect repair circuit for replacing a defective memory cell, among the plurality of volatile memory cells, with the redundancy memory cell,

wherein the defect repair circuit includes a fuse device comprising a MOSFET having a floating gate and a control gate,

said MOSFET being changed from a first threshold voltage level to a second threshold voltage level in response to an applied programming control signal, and being changed from the second threshold voltage level to the first threshold voltage level in response to an applied erase control signal, to electrically disconnect and connect the fuse device, and

wherein the MOSFET has a single polysilicon film for the floating gate, and the control gate is disposed within a well in the semiconductor substrate.

7. A defective memory cell address storage circuit for a semiconductor integrated circuit device, said circuit comprising:

a MOSFET, having a source, a drain connected to a first power supply voltage, a floating gate, and a control gate connected to a second power supply voltage, the MOSFET being configured as a fuse device for storing status information for the integrated circuit device;

an operation enabler for connecting a source of the MOSFET to a ground voltage in response to a status of an enable signal; and

a latch for latching, as the status information, a voltage level appearing at the source of the MOSFET according to a threshold voltage of the MOSFET, to store a defective memory cell address,

wherein the MOSFET has a single polysilicon film for the floating gate, and the control gate is disposed within a well in the semiconductor substrate.

8. The circuit as claimed in 7, wherein the source of the MOSFET is grounded, and wherein the first and second power supply voltages are about 3 volts and 5 volts, respectively, during a programming operation.

9. The circuit as claimed in 8, wherein the source of the MOSFET is grounded, and the first and second power supply voltages are about 5 volts and 0 volts, respectively, during an erase operation.

10. The circuit as claimed in 9, wherein the source of the MOSFET floats and both the first and second power supply voltages are each about 3 volts during a read operation.

11. The circuit as claimed in 7, wherein the operation enabler is an N-type MOS transistor.

12. The circuit as claimed in 7, wherein the latch is an inverter latch having two inverters in which an input terminal of each inverter is connected with an output terminal of the other inverter.

13. The circuit as claimed in 7, further comprising an output inverter for inverting and outputting an output of the latch.

14. A dynamic random access memory device, comprising:

a MOSFET configured as a fuse device for storing status information for the memory device, said MOSFET including,

a substrate having a first conductivity type;

a first well formed in a first portion of the substrate and having a second conductivity type;

a pocket well formed within the first well, the pocket well having the first conductivity type;

source and drain regions formed in a portion of the pocket well;

a second well formed in a second portion of the first conductive substrate, being spaced from the first well, the second well having the second conductivity type;

a control gate formed in a portion of the second well;

a floating gate of polysilicon material at least partially extending over and overlapping the control gate, extending above and overlapping portions of the pocket well and the first well in a direction approximately perpendicular to a source-drain channel between the source and the drain;

and

a tunnel oxide interposed between the floating gate and the substrate.

15. The memory device of claim 14, wherein the second conductivity type is an n-type conductivity and the first conductivity type is a p-type conductivity.